This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Twice amended) An apparatus for supporting a microprocessor development test board system in order to test for a target board, the apparatus comprising:

a micro-controller unit MCU for communicating data and control signals with respect to the target board through a multiplicity of pins;

a I/O control means for selectively outputting a RAM address, a specific function register (SFR) address and data outputted from the MCU to the target board and controlling inputted data to the MCU through the multiplicity of pins; and

means for receiving the RAM address, the SFR address and the data through the ~~plurality~~ multiplicity of pins, for providing the received data to the target board and for controlling data to be inputted to the communication means.

2. (Previously amended) The apparatus as recited in claim 1, wherein the receiving means for receiving comprises:

a port data decoder for receiving the RAM address or the SFR address and for decoding the received RAM or SFR addresses to develop a first output signal and a plurality of decoded output signals;

a controller for receiving the RAM or SFR data and the first output signal;

a first set of multiplexers for selectively transmitting the RAM or SFR data to the target board through a selected port in response to output signal from the controller and the port data decoder.

3. (Twice amended) The apparatus as recited in claim [1] 2, wherein the first set of multiplexers comprise:

a three-phase buffer responsive to the controller for outputting a plurality of buffer signals corresponding to the selected ones of the plurality of decoded output signals and the RAM or SFR data; and

a second multiplexer for selecting one of the plurality of data from the target board in response to the port data decoder.

4. (Previously canceled)

5. (Twice amended) The apparatus as recited in claim [4] 1, wherein the I/O control means comprises:

a first multiplexer having first and second input terminals and being controlled by an address selection signal, wherein the first multiplexer receives the RAM address or the SFR address at the first input terminal of the multiplexer and a program code low address at the second input terminal of the first multiplexer; and

a second multiplexer having first and second input terminals and being controlled by an MDS test signal, wherein the second multiplexer receives an output of the first multiplexer at the first input terminal of the second multiplexer and the RAM data or the SFR data at the second input terminal of the second multiplexer.

6. (Twice amended) An apparatus for supporting a microprocessor development test board system, the apparatus comprising:

a target board having a plurality of functional circuits;

a micro-controller unit MCU chip connected to the target board through a multiplicity of first pins for receiving a program codes and providing a program to the target board;

a plurality of storage blocks connected to an interface through which a programmer check up results of the ~~programs~~ program;

a decoder for receiving and decoding address signal to access one of the storage blocks;

a I/O control means connected to the ~~MUC~~ MCU chip through a multiplicity of second pins for selecting one of data transmitted through the plurality of first pins in the target board in response to the coded output signals from the decoder.

7. (Previously amended) The apparatus as recited in claim 6, wherein the I/O control means has an I/O port comprising:

a first multiplexer having first and second input terminals and being controlled by an address selection signal, wherein the first multiplexer receives the RAM address or the SFR address at the first input terminal and a program code low address at the second input terminal; and

a second multiplexer having first and second input terminals and being controlled by an MDS test signal, wherein the second multiplexer receives an output of the first multiplexer at the first input terminal and the RAM data or the SFR data at the second input terminal.

8. (Original) The apparatus as recited in claim 6, wherein the storage blocks are RAM or register blocks.

9. (Twice amended) The apparatus as recited in claim [8] 6, wherein the decoder includes:

a port data decoder for receiving a RAM or register address and for decoding the received RAM or register addresses to develop a first output signal and the coded output signals;

a controller for receiving the RAM or register data and a first output signal; and

a first set of multiplexers for selectively transmitting the RAM or register data to the target board through a selected port in response to output signal from the controller and the ort data decoder.